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REMARKS

Claims 1, 3 and 5 stand rejected under 35 U.S.C. § 102 as being anticipated by Andrews '737 ("Andrews"), and claims 2, 4 and 6 stand rejected under 35 U.S.C. § 103 as being unpatentable over Andrews. Claims 1 and 4 are independent. These rejections are respectfully traversed for the following reasons.

As a preliminary matter, Applicants note that the Examiner maintains the assertion that the two CMOS Modules of Andrews must have the same function because they have the same reference 20, in view of the requirement set forth in 37 C.F.R. 1.84(p)(4) that the same reference character must be used to designate the same part. It is respectfully submitted that the Examiner's assumption that the same part necessitates the same function is false. As is well known with electrical components, the same parts can have different functionality based on unique internal circuitry (easy example is two resistors having different resistances, equally applicable to two CMOS Modules being the same part but having different internal circuitry to function as an adder and subtractor, respectively). 37 C.F.R. 1.84(p)(4) does not require the same parts to have the same functionality, and as described on page 8, line 17 – page 9, line 14 of Applicants' specification, the same parts can have different functions. The Examiner is reminded that "inherency may not be established by probabilities or possibilities", *Scaltech Inc. v. Retec/Tetra*, 178 F.3d 1378 (Fed. Cir. 1999).

Nonetheless, in order to expedite allowance of the present application, claims 1 and 4 have been amended to include the substantive limitations of claim 2. Claims 1 and 4 each recite in pertinent part, "one signal line for simultaneously receiving both the outputs of said first and second output circuits." In contrast, Andrews merely discloses a ground line of the alleged first and second

logical circuits which does not *simultaneously* receive both the outputs of the alleged first and second output circuits in the manner set forth in claims 1 and 4.

According to an aspect of the present invention, by providing one signal line, in the case where the first logic circuit outputs a value different from the second logic circuit in a testing mode, the power supply and the ground can be short-circuited via the one signal line in both the output circuits having different voltages of "1" bit and "0" bit (e.g., the output circuit outputs a power supply voltage when the value of one bit is "1", and outputs a ground voltage when the value of one bit is "0"). Accordingly, an excessive current will flow through the signal line, thereby enabling the determination of whether the first logic circuit outputs the same or different value relative to the second logic circuit. Because the second logic circuit has the same function as the first logic circuit, when the value of the output from the first logic circuit is different from that of the second logic circuit, it can be determined that at least one of the two logic circuits is defective.

As anticipation under 35 U.S.C. § 102 requires that each and every element of the claim be disclosed, either expressly or inherently (noting that "inherency may not be established by probabilities or possibilities", *Scaltech Inc. v. Retec/Tetra*, 178 F.3d 1378 (Fed. Cir. 1999)), in a single prior art reference, *Akzo N.V. v. U.S. Int'l Trade Commission*, 808 F.2d 1471 (Fed. Cir. 1986), based on the forgoing, it is submitted that Andrews does not anticipate claim 1, nor any claim dependent thereon. The Examiner is directed to MPEP § 2143.03 under the section entitled "All Claim Limitations Must Be Taught or Suggested", which sets forth the applicable standard:

> To establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. (citing *In re Royka*, 180 USPQ 580 (CCPA 1974)).

In the instant case, the pending rejection does not "establish *prima facie* obviousness of [the] claimed invention" as recited in claims 1 and 4 because the proposed combination fails the "all the claim limitations" standard required under § 103.

Under Federal Circuit guidelines, a dependent claim is nonobvious if the independent claim upon which it depends is allowable because all the limitations of the independent claim are contained in the dependent claims, *Hartness International Inc. v. Simplimatic Engineering Co.*, 819 F.2d at 1100, 1108 (Fed. Cir. 1987). Accordingly, as claims 1 and 4 are patentable for the reasons set forth above, it is respectfully submitted that all claims dependent thereon are also patentable. In addition, it is respectfully submitted that the dependent claims are patentable based on their own merits by adding novel and non-obvious features to the combination.

Based on the foregoing, it is respectfully submitted that all pending claims are patentable over the cited prior art. Accordingly, it is respectfully requested that the rejections under 35 U.S.C. § 102/103 be withdrawn.

CONCLUSION

Having fully responded to all matters raised in the Office Action, Applicant submits that all claims are in condition for allowance, an indication for which is respectfully solicited. If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicant's attorney at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including

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extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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